AMENDMENTS TO THE CLAIMS

Please amend claims 16, 26 and 28, as set forth below. The following listing of claims is provided in accordance with 37 C.F.R. § 1.121.

1-15. (Canceled)

16. (Currently Amended) A method comprising:
fabricating a plurality of integrated circuit die on a wafer;
testing the integrated circuit die on the wafer to determine electrically good integrated circuit die;
producing a wafer map depicting the electrically good integrated circuit die; ~~and~~
grinding the wafer to a desired thickness after producing the wafer map; and
disposing an adhesive material onto only the electrically good integrated circuit die in accordance with the wafer map.

17. (Previously Presented) The method, as set forth in claim 16, wherein disposing the adhesive comprises disposing an adhesive tape onto the electrically good integrated circuit die in accordance with the wafer map.

18. (Previously Presented) The method, as set forth in claim 16, wherein disposing the adhesive comprises disposing an adhesive paste onto the electrically good integrated circuit die in accordance with the wafer map.

19-21. (Canceled)

22. (Previously Presented) The method, as set forth in claim 16, comprising forming an integrated circuit package comprising the electrically good integrated circuit die.

23. (Previously Presented) The method, as set forth in claim 16, comprising forming a board on chip package comprising the electrically good integrated circuit die.

24. (Previously Presented) The method, as set forth in claim 16, comprising forming a lead on chip package comprising the electrically good integrated circuit die.

25. (Previously Presented) The method, as set forth in claim 16, wherein the acts are performed in the recited order.

26. (Currently Amended) A method comprising:

identifying electrically good integrated circuit die on a wafer; ~~and~~

grinding the wafer to a desired thickness after identifying the electrically good integrated circuit die on the wafer; and

disposing an adhesive material onto only the electrically good integrated circuit die on the wafer after grinding the wafer to the desired thickness.

27. (Previously Presented) The method, as set forth in claim 26, comprising producing a wafer map depicting the electrically good integrated circuit die.

28. (Currently Amended) The method, as set forth in claim 26, wherein identifying comprises identifying the electrically good integrated circuit die by probing the wafer and producing ~~using~~ a wafer map depicting the electrically good integrated circuit die.

29. (Previously Presented) The method, as set forth in claim 26, wherein disposing the adhesive material comprises disposing an adhesive tape.

30. (Previously Presented) The method, as set forth in claim 26, wherein disposing the adhesive material comprises disposing an adhesive paste.

31. (Previously Presented) The method, as set forth in claim 26, comprising forming an integrated circuit package comprising the electrically good integrated circuit die.

32. (Previously Presented) The method, as set forth in claim 26, comprising forming a board on chip package comprising the electrically good integrated circuit die.

33. (Previously Presented) The method, as set forth in claim 26, comprising forming a lead on chip package comprising the electrically good integrated circuit die.